New TRT Hardware Interlock Design

Hal Evans and Paul Smith

1) New (simplified) TRT-HWI Design

2) First Tests

3) Operations and Risk Analysis

4) More Information
   • 1st Proposal: talk on 14 November, 2006
Simplified Philosophy

VERY useful discussion in 14-Nov. Meeting

1) Primary mechanism for cutting power to TRT is DCS
   • TRT-HWI should act only if DCS fails

2) No need for redundant NTC monitoring
   • DCS takes care of this, monitor only TRT-HWI elements

3) DCS controls power to individual channels
   • NCTs remain powered even if channel is off
   • TRT-HWI can remain continuously operational

4) Local trip capability (at PPs) desirable
New Design

- No programmable logic in system
- Thresholds set using socketed resistors
  Delay with socketed RC circuit
- Local Trip output from Comparator Boards (barrel/endcap)
Location and Board Counts

UX15 – A side

1 Logic Board near TRT LV/HV Racks

*64 Comp Board to Logic Board Cables
• ethernet style cables
• 1 per comparator board
• run these USA15-to-UX15 (~100m)

<table>
<thead>
<tr>
<th>Location (per side)</th>
<th>PP2 Boxes</th>
<th>NTCs (bar+end)</th>
<th>Comp Boards</th>
<th>Output Cables*</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>8</td>
<td>8 + 20</td>
<td>8</td>
<td>8</td>
</tr>
<tr>
<td>2</td>
<td>5</td>
<td>8 + 20</td>
<td>5</td>
<td>5</td>
</tr>
<tr>
<td>3</td>
<td>5</td>
<td>8 + 20</td>
<td>5</td>
<td>5</td>
</tr>
<tr>
<td>4</td>
<td>8</td>
<td>8 + 20</td>
<td>8</td>
<td>8</td>
</tr>
<tr>
<td>5</td>
<td>3</td>
<td>8 + 20</td>
<td>3</td>
<td>3</td>
</tr>
<tr>
<td>6</td>
<td>3</td>
<td>8 + 20</td>
<td>3</td>
<td>3</td>
</tr>
</tbody>
</table>

TOTAL 64

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Comparator Board

Comparator Circuit (Bar & End Sums)

- individual chan LEDs & filtering

Adjustable NTC Thresholds (socketed R)

Barrel & Endcap Sums to Logic Board (twisted pairs, tunable filtering)

"current loop" output

"zero state" output current
Comparator (Local Trip)

Adjustable Bar & End
NTC Mult Thresholds
(socketed R)

Local Trip (Bar & End)
Indicator LEDs

Open Drain Output
(combine with “T”)

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TRT Hardware Interlock Proposal v.2 : 26-Jan-07
Comparator Board Layout

 disable switches

1\textsuperscript{st} Level Comparators  LEDs & filters  2\textsuperscript{nd} Level Comparators

Barrel
NTC
Input

3"

EndCap
NTC
Input

5"

Bar/End
thresh R's

still a few filtering R's & C's to add (Rick's comments)
Response at Instr. Amp. Output
(Probe 1 – No Noise)

Noise Sensitivity

Response at Instr. Amp. Output
(Probe 1 – No Noise)
### Operations & Risk Analysis

<table>
<thead>
<tr>
<th>Situation</th>
<th>Cause / Consequence</th>
<th>TRT-HWI Action / Risk</th>
</tr>
</thead>
<tbody>
<tr>
<td>power-on state</td>
<td>fully determined by NTCs</td>
<td>no logic to configure in TRT-HWI system</td>
</tr>
<tr>
<td>temp too high</td>
<td>$n$ NTCs over threshold</td>
<td>DCS turns off chan's, NTCs stay powered</td>
</tr>
<tr>
<td>temp too high &amp; DCS fails</td>
<td>$n$ NTCs over threshold</td>
<td>trip</td>
</tr>
<tr>
<td>open / shorted NTC</td>
<td>$Vin=2.5$ (T=0) / $Vin=0$ (T=high)</td>
<td>nothing / trip, disable NTC on Comp Brd</td>
</tr>
<tr>
<td>changed NTC response</td>
<td>$T = \text{low} / T = \text{high}$</td>
<td>monitor drift in DCS, adjust thresh. R</td>
</tr>
<tr>
<td>TTC or TTC cable broken</td>
<td>$Vin=0$</td>
<td>trip</td>
</tr>
<tr>
<td>Comp out cable broken</td>
<td>detected at Logic Board</td>
<td>trip, temporarily disable Comp Brd Input</td>
</tr>
<tr>
<td>Logic out cable broken</td>
<td>$Vout=0$ to rack</td>
<td>trip</td>
</tr>
<tr>
<td>transient noise</td>
<td>NTC(s) temporarily over thresh</td>
<td>protected against by trip delay</td>
</tr>
<tr>
<td>disabled channels</td>
<td>forget to re-enable</td>
<td>difficult to spot, check switches on Comp brds</td>
</tr>
<tr>
<td>disable Comp Board</td>
<td>broken &amp; waiting for access</td>
<td>switch on Logic Board</td>
</tr>
<tr>
<td>disable Logic Board output</td>
<td>commissioning / testing</td>
<td>switch on Logic Board</td>
</tr>
<tr>
<td>DSS trips TRT</td>
<td>when would this happen ?</td>
<td>need to reset TRT-HWI</td>
</tr>
</tbody>
</table>

1) Comments from Group  

end Jan

2) Produce Prototype Comparator Boards  
   - fabricate all PCBs  
   - assemble ~5 in house  

end Feb

3) Finalize Logic Board Design (in parallel)  
   - create operating instructions  

end Mar

4) Test Comparator Boards at CERN  
   - use Local Trip feature for commissioning  

end Apr

5) Produce/Test Final Boards  

end June