TRT Hardware Interlock Proposal

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1) Need for a Hardware Interlock
2) Fitting into the Overall ATLAS Safety Scheme
3) Proposed Hardware and Algorithms
4) Thoughts and Questions on Trip Recovery
Thanks and Warning!

Extremely Helpful Advice from


Warning

- these are still preliminary ideas
- our (Hal & Paul) assumptions/understanding may be incorrect
  - (despite the efforts of those above to educate us)

Input from Everyone is Very Welcome!
Why a HW Interlock?

- Cooling Incidents in SR (not acted on by DCS)
  - April, 2006 electronics to ~100° for ~12 hours
  - 2004 beam test

- July, 2006 Review
  - “The TRT subdetector should study the possibility of an HW interlock scheme (and implement it), in order to avoid overheating of detector elements, possibly using the same tools as the silicon detectors.”
  - “Any abnormal and potentially dangerous situation caused by the malfunction of a service should, as much as possible, at either DSS or hardware interlock level be detected by an independent sensor directly measuring the result of this service…”

- Design “fool-proof” TRT Temperature-based Interlock
1) DCS (Detector Control System)
   - control, monitor and operate subdetectors
   - flexible but complicated ⇒ possible to inadvertently disable

2) DSS (Detector Safety System – ATLAS wide)
   - for example: drop rack power if 5 minutes without cooling
   - less flexible ⇒ safer, but not tailored to specific needs

3) TRT HW Interlock (Subdetector Specific)
   - option of “last resort” ⇒ limited flexibility
   - acts based on temperature measurements
   - impossible (very difficult) to disable by mistake
System Architecture

NTC Thermistors from new TTC PP2 Boards

Two New Boards to Build

1) Comparator Board  compares NTCs to threshold
2) Logic Board  determines if trip condition is met

System Architecture

[Diagram showing the flow of power from Barrel TTC and End Cap TTC to Compare, then to Logic Box, with connections to USA15 and MARATON Supplies]
**Location and Board Counts**

**UX15 – A side**

1 Logic Board near TRT LV/HV Racks

- **64** Comp Board to Logic Board Cables
  - ethernet style cables
  - 1 per comparator board
  - NEED to run these USA15-to-UX15

<table>
<thead>
<tr>
<th>Location (per side)</th>
<th>PP2 Boxes</th>
<th>NTCs (bar+end)</th>
<th>Comp Boards</th>
<th>Output Cables*</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>8</td>
<td>8 + 20</td>
<td>8</td>
<td>8</td>
</tr>
<tr>
<td>2</td>
<td>5</td>
<td>8 + 20</td>
<td>5</td>
<td>5</td>
</tr>
<tr>
<td>3</td>
<td>5</td>
<td>8 + 20</td>
<td>5</td>
<td>5</td>
</tr>
<tr>
<td>4</td>
<td>8</td>
<td>8 + 20</td>
<td>8</td>
<td>8</td>
</tr>
<tr>
<td>5</td>
<td>3</td>
<td>8 + 20</td>
<td>3</td>
<td>3</td>
</tr>
<tr>
<td>6</td>
<td>3</td>
<td>8 + 20</td>
<td>3</td>
<td>3</td>
</tr>
</tbody>
</table>

**TOTAL** 64

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TRT Hardware Interlock Proposal
Comparator Board

NTC Inputs
- split from TTC ELMBs

Data I/O
- 4 LVDS pairs on ethernet cable

Data Out: 48 bits / cycle
- 28 NTC thresh compare bits
- 16 current DAC thresholds
- 4 framing (hard-wired)

Data In: 44 bits / cycle
- NTC test patterns → Data Out
- DAC values for thresholds
NTC Pickoff

[Diagram of circuit with labels:
- NTC Thermistor (47 KΩ @ 25°C)
- +2.5 V Ref
- 470 KΩ
- ELMB
- PP GND
- PP2
- TTC
- 100 Ω
- 22 MΩ
- DAC
- +3.3 V Ref
- (bias: 25 nA)
- Comparator Board

Graph showing the voltage [V] as a function of temperature [°C].]
## Comparator Board Components

<table>
<thead>
<tr>
<th>Part No.</th>
<th>Function</th>
<th>Rad Tolerance</th>
</tr>
</thead>
<tbody>
<tr>
<td>Micrel 29151</td>
<td>Voltage Regulator</td>
<td>in CERN database</td>
</tr>
<tr>
<td>DS90LV048A</td>
<td>LVDS Receiver</td>
<td>in CERN database</td>
</tr>
<tr>
<td>DS90LV047A</td>
<td>LVDS Driver</td>
<td>in CERN database</td>
</tr>
<tr>
<td>OPA336</td>
<td>Op Amp</td>
<td>in CERN database</td>
</tr>
<tr>
<td>LM339</td>
<td>Comparator</td>
<td>SET &amp; TID (100 KRad) qualified</td>
</tr>
<tr>
<td>74AC299</td>
<td>Shift Register</td>
<td>100 – 300 Krad</td>
</tr>
<tr>
<td>resistors, capacitors</td>
<td>Various</td>
<td>---</td>
</tr>
<tr>
<td>SS-6488-NF-RMK</td>
<td>RJ45 Output Connector</td>
<td>---</td>
</tr>
<tr>
<td>ERNI-124044</td>
<td>NTC Input Connector</td>
<td>---</td>
</tr>
<tr>
<td>Molex 70533</td>
<td>Power Socket</td>
<td>---</td>
</tr>
<tr>
<td>Molex 50-57-9402</td>
<td>Power Plug</td>
<td>---</td>
</tr>
</tbody>
</table>
Comparador Board Layout

Ready for Prototyping

Comparators   Shift Registers   Barrel Threshold DAC

from Barrel TTC

from Endcap TTC

3.0"

4.5"

Endcap Threshold DAC

Power In

Clock, Load, Data, In/Out
Safety Features

- Watchdog Circuit
- Configuration ONLY thru JTAG
  - locally in USA15
- NO Remote Disable or Reset
- Time above threshold requirement
  - reduced sensitivity to transients

Monitoring

- info to DCS to be decided
  - watchdog, state, channel status...
- also available locally thru JTAG

Testing (via JTAG)

- fixed/random test patterns to Comp Boards for readback

1) LVDS Receivers
2) Logic FPGA → Flexibility
3) Configuration: PROM or JTAG
4) Monitoring: ELMB, JTAG, LEDs
5) Relays: USA15 Racks / Maratons?
6) Manual Reset Button

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Possible Algorithm

Comparator Board

Input

NTCs over Thresh
in Regions

Time Over
Limit

Alarm
Generation

- Comparator bit stream
- Comparator bit stream

MUX

address counter

Channel Weight LUT
64 x 28 x 4b x N

accumulator

limit comp

time counter

Alarm Logic

StateMachine

watchdog bit

configuration

PROM/JTAG

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TRT Hardware Interlock Proposal
## Algorithm Description

<table>
<thead>
<tr>
<th>Element</th>
<th>Description</th>
</tr>
</thead>
</table>
| **Channel Input**  | o address counter increments thru 28 channels  
                        o look-up-memory contains weight for each channel  
                        o weight output if channel above threshold                                                                                       |
| **Accumulators**   | o sum weights in different regions                                                                                                           |
| **Limits**         | o “trip bit” set if region accumulator sum over limit for pre-set period of time                                                           |
| **Alarm**          | o pre-defined combination of region trip-bits set  
                        o single? or multiple? trip output signals                                                                                 |
| **Configuration**  | o normally stored in on-board PROM  
                        o can be loaded *in situ* by JTAG                                                                                                 |
| **State Machine**  | o controls operation of entire system  
                        o monitors status – sets watchdog bit  
                        (reload configuration from PROM...)  
                        o watchdog compares *e.g.* its NTC threshold set with values read from Comparator Boards in data stream |
Trip Recovery

Assume power is cut at rack level (entire PP Location)

- possible by: DCS, DSS, TRT-HW
- no signals from NTCs, no data to Logic Board
- need to reset all affected systems (DCS, DSS, TRT-HW)

Two Scenarios

1) DCS or DSS initiates Trip  TRT-HW should *not* Trip
2) TRT-HW initiates Trip  need to Reset in USA15

Possible TRT-HW States (Logic Board)

- **OK**  NTC data good; trip condition not met  do not trip
- **WAIT**  power off at Comp Board(s); monitor data  do not trip
- **TRIP**  NTC data good; trip condition met  Trip
- **DISABLED**  monitor data  do not trip
Conclusions

TRT Hardware Interlock: Last Line of Defense

- uses existing temperature monitoring
- add 64 ethernet style cables: USA15 to Patch Panel Locations
- simple system – very difficult to inadvertently disable
- trip requires programmable set of NTCs over threshold for an extended time interval
- watchdog restarts/reloads if necessary

Design Well Advanced

- Comparator Board ready for prototyping
- Logic Board ready to start schematics/layout

Comments/Suggestions Very Welcome!