0) Read/Re-Read/Review Chapter 4, sections 4.5-4.8.

1) Assume that you have a CPU that utilizes 5 stages with the following latencies:

<table>
<thead>
<tr>
<th>Fetch (IF)</th>
<th>Decode (ID)</th>
<th>Execute (ALU)</th>
<th>Memory (Mem)</th>
<th>Write Back (WB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>300 ps</td>
<td>400 ps</td>
<td>350 ps</td>
<td>550 ps</td>
<td>100 ps</td>
</tr>
</tbody>
</table>

Assume that when pipelining each stage costs an extra 20ps for the registers between pipeline stages.

a) For a non-pipelined processor, what is the latency of an instruction? What is the clock rate?

b) For a pipelined processor (5 stages), what is the latency of an instruction? What is the clock rate?

c) If you could split one of the pipeline stages into 2 equal halves, which one would you choose? What would be the new latency and clock rate with this change?

2) Consider the following sequence of instructions:

1. lw $s2, 0($s1)
2. lw $s1, 40($s6)
3. sub $s6, $s1, $s2
4. add $s6, $s2, $s2
5. or $s3, $s6, $zero
6. sw $s6, 50($s1)

   a) List all of the data dependencies. The first is given to you - use this format when listing all of the others.

   3 depends on 1 ($s2)

   b) Assume that a 5-stage MIPS pipeline is being used with no forwarding and each stage takes 1 cycle. Instead of inserting NOPS you let the process stall on hazards. How many times does the processor stall? How long is each stall (in cycles)? What is the execution time (in cycles) for the entire program?

   c) Assume that full-forwarding has been added. write the program with NOPs to eliminate the hazards. Note: Delay slots are not used.

**TURN IN:**

- Create a Word document (.docx format) that contains the answers to the problems. Upload this file to the appropriate Assignments folder in Canvas.
- Work is due at 9:35am on the due date.